L Number	Hits	Search Text	DB	Time stamp
1	12	(H adj Hayashi) and TFT	USPAT; US-PGPUB	2003/02/21 11:52
2	1551	TFT and laser and (crystalline with silicon)	USPAT; US-PGPUB	2003/02/21 12:16
3	718	(TFT and laser and (crystalline with silicon)) not (semiconductor adj energy adj laboratory)	USPAT; US-PGPUB	2003/02/21 12:17
4	571	((TFT and laser and (crystalline with silicon)) not (semiconductor adj energy adj laboratory)) and (source or drain) and channel	USPAT; US-PGPUB	2003/02/21 12:17
5	558	(((TFT and laser and (crystalline with silicon)) not (semiconductor adj energy adj laboratory)) and (source or drain) and channel) and gate	USPAT; US-PGPUB	2003/02/21 12:17
6	466	((((TFT and laser and (crystalline with silicon)) not (semiconductor adj energy adj laboratory)) and (source or drain) and channel) and gate) and (doping or implanting)	USPAT; US-PGPUB	2003/02/21 12:17
7	97	TFT and laser and (crystalline with silicon)	EPO; JPO; DERWENT; IBM_TDB	2003/02/21 12:08
8	1578	438/158,149,161,166.ccls.	USPAT; US-PGPUB	2003/02/21 12:18
9	1284	438/158,149,161,166.ccls. not (semiconductor adj energy adj laboratory)	USPAT; US-PGPUB	2003/02/21 12:19
10	942	(438/158,149,161,166.ccls. not (semiconductor adj energy adj laboratory)) and (source or drain) and channel	USPAT; US-PGPUB	2003/02/21 12:19
11	588	((438/158,149,161,166.ccls. not (semiconductor adj energy adj laboratory)) and (source or drain) and channel) and (doping or implanting)	USPAT; US-PGPUB	2003/02/21 12:19
12	586	(((438/158,149,161,166.ccls. not (semiconductor adj energy adj laboratory)) and (source or drain) and channel) and (doping or implanting)) and gate	USPAT; US-PGPUB	2003/02/21 12:19
13	1434	257/59,69,72.ccls.	USPAT; US-PGPUB	2003/02/21 12:18
14	1155	257/59,69,72.ccls. not (semiconductor adj energy adj laboratory)	USPAT; US-PGPUB	2003/02/21 12:19
15	825	(257/59,69,72.ccls. not (semiconductor adj energy adj laboratory)) and (source or drain) and channel	USPAT; US-PGPUB	2003/02/21 12:19
16	401	((257/59,69,72.ccls. not (semiconductor adj energy adj laboratory)) and (source or drain) and channel) and (doping or implanting)	USPAT; US-PGPUB	2003/02/21 12:19
17	398	(((257/59,69,72.ccls. not (semiconductor adj energy adj laboratory)) and (source or drain) and channel) and (doping or implanting)) and gate	USPAT; US-PGPUB	2003/02/21 12:19

DOCUMENT-IDENTIFIER: US 20020072157 A1

TITLE: SEMICONDUCTOR DEVICE HAVING A SEMICONDUCTOR THIN FILM CONTAINING LOW CONCENTRATION OF UNBOUND HYDROGEN ATOMS AND METHOD OF MANUFACTURING THE SAME

---------- KWIC ---------

[0030] According to a fifth aspect of the invention, a method of manufacturing a thin film transistor comprises the steps of: forming a gate electrode on a surface of a substrate; forming a gate insulating film and a non-**crystalline** **silicon** film in the described order over the substrate so as to cover the gate electrode; decreasing the density of hydrogen atoms, which are contained in the non-**crystalline silicon** film, by removing the hydrogen atoms from the non-**crystalline silicon** film by an annealing process; forming a polysilicon film by polycrystallizing the non-**crystalline silicon** film by another annealing process; patterning the polysilicon film in a predetermined shape and then forming an impurity-doped region at a predetermined area in the patterned polysilicon film; after the forming of the impurity-doped region, forming a **silicon** nitride film so as to cover the patterned polysilicon film by plasma CVD and then treating the substrate, on which the polysilicon film and the **silicon** nitride film have been formed, with a thermal annealing process under nitrogen atmosphere; after the thermal annealing process, removing selected portions of the **silicon** nitride film in such a manner that a surface of the impurity-doped region in the polysilicon film is exposed; and forming a source

electrode and a drain electrode in the exposed portions of the impurity-doped region to thereby connect the source electrode and the drain electrode to the impurity-doped region at their corresponding portions.

[0031] By this method, it is possible to obtain a polysilicon film by polycrystallizing the non-**crystalline silicon** film, which defines the active region of a thin film transistor, and to prevent the density of the hydrogen atoms contained in the obtained polysilicon film becoming excessive. Further, the thermal annealing process causes an appropriate quantity of the hydrogen atoms, which had been contained in the silicon nitride film, to move into the polysilicon film to terminate the dangling bonds in the polysilicon film, thus improving the electrical characteristics of the semiconductor device employing the polysilicon film.

[0045] In FIG. 2E, a photoresist 30 larger than the gate electrode 11 is formed at least in a channel length direction (horizontally in FIG. 2E), and then, with the photoresist 30 as a mask, ion **doping** of phosphor (P) is carried out with respect to the p-Si film 13 at a high dosage of approximately 10.sup.15 to dope the entire region of the p-Si film 13 except the area covered with the photoresist 30 at a high density (N.sup.+). At that time, in the area beneath the photoresist 30, the lightly doped region (N.sup.-) and the channel region (N.sup.+), which were formed in the previous process step of FIG. 2D, remain. As a result, after the high-density ion **doping,** an LDD structure is formed in which high-doped source and drain regions 13S, 13D exist one on each side of the channel region 25 so as to keep a lightly doped LD region 13LD between the high-doped source region 13S and the channel region 25 and

a lightly doped LD
region 23LD between the high-density drain region 13D and the channel region
25.

11. A method of manufacturing a thin film transistor, comprising the steps of:
(a) forming a gate electrode on a surface of a substrate;
(b) forming a gate
insulating film and a non-**crystalline silicon** film in the described order over
the substrate so as to cover the gate electrode; (c) decreasing the density of
hydrogen atoms, which are contained in the non-**crystalline silicon** film, by
removing the hydrogen atoms from the non-**crystalline silicon** film by an
annealing process; (d) forming a polysilicon film by polycrystallizing the
non-**crystalline silicon** film by another annealing process;
(e) patterning the
polysilicon film in a predetermined shape and then forming an impurity-doped
region at a predetermined area in the patterned polysilicon film; (f) after
said forming of the impurity-doped region, forming a silicon nitride film so as
to cover the patterned polysilicon film by plasma CVD and then treating the
substrate, on which the polysilicon film and the silicon nitride film have been
formed, with a thermal annealing process; (g) after said thermal annealing
process, removing selected portions of the silicon nitride film in such a
manner that a surface of the impurity-doped region in the polysilicon film is
exposed; and (h) forming a source electrode and a drain electrode in the
exposed portions of the impurity-doped region to thereby connect the source
electrode and the drain electrode to the impurity-doped region at their
corresponding portions.

US-PAT-NO: 5290712

DOCUMENT-IDENTIFIER: US 5290712 A

TITLE: Process for forming crystalline semiconductor film

---------- KWIC ---------

Heretofore, a process for solid phase growth of a crystalline film by annealing an amorphous thin film formed in advance on a substrate at a lower temperature than the melting point has been proposed as one of processes in the field of crystal formation technology to make a crystalline film grow on a substrate such as an amorphous substrate. For example, a process for formation of crystal by annealing an amorphous Si film having thickness of about 100 nm formed on the surface of amorphous SiO.sub.2 in a N.sub.2 atmosphere at 600.degree. C., thereby crystallizing the amorphous Si thin film to obtain a polycrystalline film having grain sizes of about 5 pm is reported [T. Noguchi, **H. Hayashi** and H. Ohshima, 1987, Mat. Res. Soc. Symp. Proc., 106, Polysilicon and Interfaces, 293, (Elsevier Science Publishing, New York 1988)].
Since the surface of the polycrystalline film obtained by the process remains flat, it is possible to form electronic devices such as MOS transistors or diodes thereon. Furthermore, the average grain sizes of the polycrystalline film are larger than those of ordinary polycrystalline film obtained by LPCVD process, thus the devices formed with the polycrystalline film have a relatively high performance.

L Number	Hits	Search Text	DB	Time stamp
1	36	TFT and (RTA same (crystalline with silicon))	USPAT; US-PGPUB	2003/02/21 15:28
2	14	(TFT and (RTA same (crystalline with silicon))) and oxidizing	USPAT; US-PGPUB	2003/02/21 15:28
3	323	(BCB with (insulating or insulative or insulator or dielectric)) and TFT	USPAT; US-PGPUB	2003/02/21 16:23
4	247	((BCB with (insulating or insulative or insulator or dielectric)) and TFT) not (semiconductor adj energy)	USPAT; US-PGPUB	2003/02/21 16:24
5	55	(((BCB with (insulating or insulative or insulator or dielectric)) and TFT) not (semiconductor adj energy)) and @ad<=19990820	USPAT; US-PGPUB	2003/02/21 16:48
6	7	TFT and (amorphous adj silicon) and ((contaminants with (insulating or insulative or insulator or dielectric)) same hydrogen)	USPAT; US-PGPUB	2003/02/21 17:08
9	100	TFT and (amorphous adj silicon) and ((oxygen with (insulating or insulative or insulator or dielectric)) same hydrogen)	USPAT; US-PGPUB	2003/02/21 17:09
10	259	TFT and (amorphous adj silicon) and ((oxygen with (insulating or insulative or insulator or dielectric)) same plasma)	USPAT; US-PGPUB	2003/02/21 17:09
11	0	TFT and (amorphous adj silicon) and ((oxygen with (insulating or insulative or insulator or dielectric)) same ((active adj hydrogen) with plasma))	USPAT; US-PGPUB	2003/02/21 17:10
12	13	TFT and (amorphous adj silicon) and ((oxygen with (insulating or insulative or insulator or dielectric)) same (active adj hydrogen))	USPAT; US-PGPUB	2003/02/21 17:12
13	0	TFT and (amorphous adj silicon) and ((oxygen with (insulating or insulative or insulator or dielectric)) same (active adj hydrogen))	EPO; JPO	2003/02/21 17:12
14	0	TFT and ((oxygen with (insulating or insulative or insulator or dielectric)) same (active adj hydrogen))	EPO; JPO	2003/02/21 17:12
15	13	TFT and ((oxygen with (insulating or insulative or insulator or dielectric)) same (active adj hydrogen))	USPAT; US-PGPUB	2003/02/21 17:13
16	19	((oxygen with (insulating or insulative or insulator or dielectric)) same (active adj hydrogen))	USPAT; US-PGPUB	2003/02/21 17:15
17	6	(((oxygen with (insulating or insulative or insulator or dielectric)) same (active adj hydrogen))) not (TFT and ((oxygen with (insulating or insulative or insulator or dielectric)) same (active adj hydrogen)))	USPAT; US-PGPUB	2003/02/21 17:14
18	175	((oxygen with (insulating or insulative or insulator or dielectric)) same (plasma with hydrogen))	USPAT; US-PGPUB	2003/02/21 17:15
19	31	(((oxygen with (insulating or insulative or insulator or dielectric)) same (plasma with hydrogen))) and tft	USPAT; US-PGPUB	2003/02/21 17:16
20	31	((((oxygen with (insulating or insulative or insulator or dielectric)) same (plasma with hydrogen))) and tft) not (TFT and ((oxygen with (insulating or insulative or insulator or dielectric)) same (active adj hydrogen)))	USPAT; US-PGPUB	2003/02/21 17:16

US-PAT-NO: 5685949

DOCUMENT-IDENTIFIER: US 5685949 A

TITLE: Plasma treatment apparatus and method

---------- KWIC ---------

According to the plasma oxidation process, oxygen molecules react more than
oxygen radicals with the **hydrogen** bonds of the silicon in the silicon oxide
film. Thus, it is possible to increase the dielectric strength in the silicon
oxide film more than that of the conventional heat oxidation. For example, if
a silicon oxide film having a thickness of 200 Angstroms is formed within 100%
oxygen atmosphere under normal pressure without plasma, the dielectric strength
becomes 8-10 MV/cm. In the presence of a plasma, however, the dielectric
strength increases up to 10-12 MV/cm.

US-PAT-NO: 5637512

DOCUMENT-IDENTIFIER: US 5637512 A

TITLE: Method for fabricating a thin film semiconductor device

---------- KWIC ---------

Conventionally in fabricating such thin film transistor, thermal oxidation has
been used to form a gate insulating layer. That is, to form the gate
insulating layer after the formation of a channel silicon layer, a substrate is
inserted into an oxidizing ambient atmosphere containing **oxygen,** (O.sub.2),
laughing gas (N.sub.2 O), vapor (H.sub.2 O), etc. to raise its temperature to
800.degree. about 1100.degree. C. and partially oxidize the channel silicon
layer. On the other hand, various processes have been tried in fabricating
thin film semiconductor devices using polycrystalline silicon at maximum
processing temperatures below about 600.degree. C. at which inexpensive
ordinary glass can be used. They are exemplified by the process in which a
channel semiconductor layer is formed as-deposited polycrystalline silicon
which is prepared by low pressure chemical vapor deposition (LPCVD) with the
deposition temperature of about 600.degree. C. or more, and then a gate
insulating film is formed by electronic cyclotron resonance plasma CVD
(ECR-PECVD) and is further subjected to hydrogenation by e.g., **hydrogen plasma**
radiation. They are also exemplified by the process in which an amorphous
silicon thin film is deposited on a channel semiconductor layer, then is

heat-treated for about 24 hours at 600.degree. C., and then a gate insulating
film is formed by atmospheric pressure chemical vapor deposition (APCVD) and is
subjected to hydrogen treatment (Japanese J. Appl. Phys. 30L 84, uL91).

US-PAT-NO: 5619044

DOCUMENT-IDENTIFIER: US 5619044 A

TITLE: Semiconductor device formed with seed crystals on a layer thereof

---------- KWIC ---------

Then, as shown in FIG. 4D, an interlayer insulating film 118 made of silicon oxide or silicon nitride having a thickness of about 6000 .ANG. is formed by a plasma CVD method, or the like. In the case of forming a silicon oxide film, if the silicon oxide film is formed by a method for dissolving TEOS with **oxygen** by the RF plasma CVD, or by a method for dissolving TEOS with ozone gas by the low-pressure plasma CVD or by the ambientpressure CVD, then a satisfactory interlayer insulating film excellent in the step coverage may be obtained. In the case of forming the silicon nitride film, if the film is deposited by the plasma CVD method using SiH.sub.4 and NH.sub.3 as source gases, then **hydrogen** may be supplied to the interfaces between the active region and the gate insulating film and the dangling bonds in the crystalline silicon film can be terminated with **hydrogen**, thereby improving the characteristics of the TFT.

L Number	Hits	Search Text	DB	Time stamp
1	36	TFT and (RTA same (crystalline with silicon))	USPAT; US-PGPUB	2003/02/21 15:28
2	14	(TFT and (RTA same (crystalline with silicon))) and oxidizing	USPAT; US-PGPUB	2003/02/21 15:28

US-PAT-NO: 5851860

DOCUMENT-IDENTIFIER: US 5851860 A

TITLE: Semiconductor device and method for producing the same

---------- KWIC ---------

However, the substrate must be heated at a high temperature of 1000.degree. C. or more in order to perform this thermally **oxidizing** process, so that this process is unsuitable for a TFT to be produced on an inexpensive glass substrate. Even if a thermally oxidized film is formed by using a highly heat-resistant substrate such as a quartz substrate, a silicon film to be subjected to the thermal oxidization is not a single crystalline silicon film but a crystalline silicon film. Accordingly, the insulation properties of the oxidized silicon film to be obtained by **oxidizing** the crystalline silicon film are poor, and therefore the oxidized silicon film is far from being usable as a gate insulating film.

In the above-described examples, heat treatment is conducted using an excimer laser (or pulse laser) beam in order to promote the crystallinity of the **crystalline silicon** film. Other kinds of laser beams (e.g., a continuously oscillating Ar laser beam) can also be used for conducting a similar heat treatment. A so-called rapid thermal annealing (**RTA**) or a rapid thermal process (RTP) for heating a sample up to a temperature of 1000.degree. to 1200.degree. C. (i.e., the temperature of a silicon monitor) in a short period

of time by using an intense light emitted from an infrared light and a flash
lamp can also be utilized.

US-PAT-NO: 6462798

DOCUMENT-IDENTIFIER: US 6462798 B1

TITLE: Multi-domain liquid crystal display device

---------- KWIC ---------

On the common electrode 17, dielectric frames 53 are formed by depositing photosensitive material and patterning in various shapes using photolithography. The **dielectric** frame 53 includes material of which **dielectric** constant is same or smaller than that of the liquid crystal, and the **dielectric** constant thereof is preferably below 3, for example, photoacrylate or **BCB** (BenzoCycloButene).

10. The multi-domain liquid crystal display device according to claim 7, wherein said **dielectric** frame includes a material selected from the group consisting of photoacrylate and **BCB** (BenzoCycloButene).

13. The multi-domain liquid crystal display device according to claim 6, wherein said **dielectric** frame includes a material selected from the group consisting of photoacrylate and **BCB** (BenzoCycloButene).

DOCUMENT-IDENTIFIER: US 20010046000 A1

TITLE: A METHOD FOR MANUFACTURING AN LCK IN WHICH A PHOTORESIST LAYER IS AT
LEAST 1.2 TIMES THICKER THAN THE PASSIVATION LAYER

---------- KWIC ---------

[0018] In the above mentioned conventional method, because the passivation
layer 26 has a lower **dielectric** constant (lower than 3.0) than the inorganic
material and forms an organic **insulating** layer(**BCB**) which can even a surface
property thereof, the pixel electrode 4 disposed on the passivation layer can
be overlapped with the data line 15 so that the aperture ratio can be
maximized.